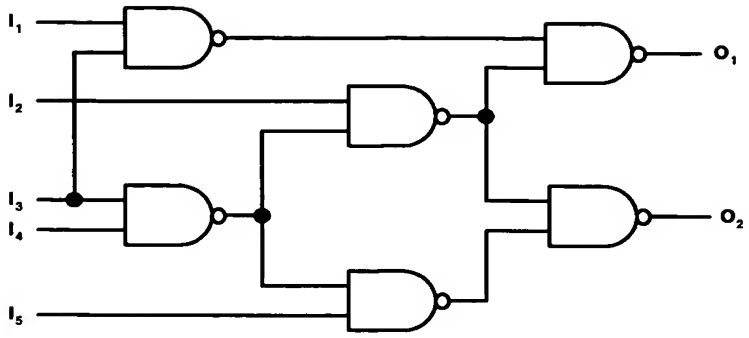


Fig. 1a

	I_1	I_2	I_3	I_4	I_5
t_1	0	1	1	0	X
t_2	X	0	0	X	0
t_3	X	X	1	1	1
t_4	X	1	1	1	X
t_5	0	0	1	X	X
t_6	X	0	0	X	1
t_7	X	1	0	1	X
t_8	1	0	0	X	X
t_9	1	0	1	X	X
t_{10}	X	1	0	X	0

Fig. 1b

	I_1	I_2	I_3
t_1	0	1	1
t_2	0	0	0
t_3	1	X	1
t_4	1	1	1
t_5	0	0	1
t_6	1	0	0
t_7	1	1	0
t_8	1	0	0
t_9	1	0	1
t_{10}	0	1	0

Fig. 1c

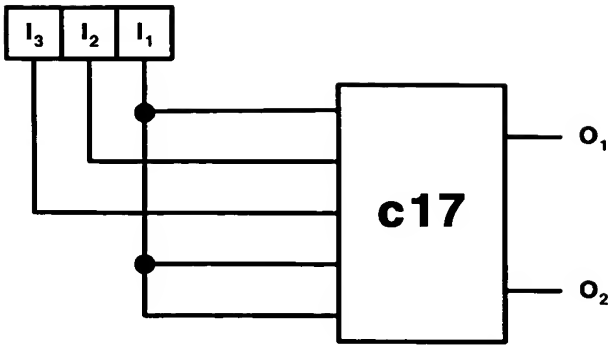


Fig. 2

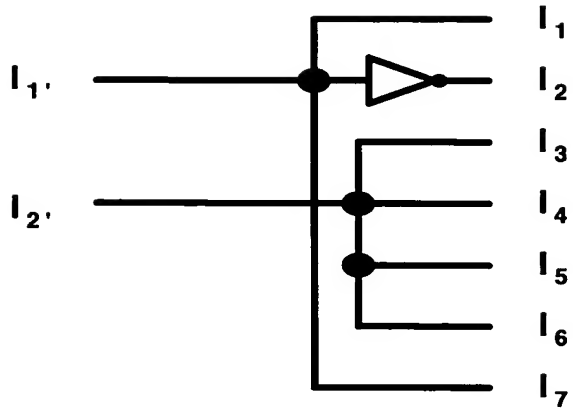


Fig. 3

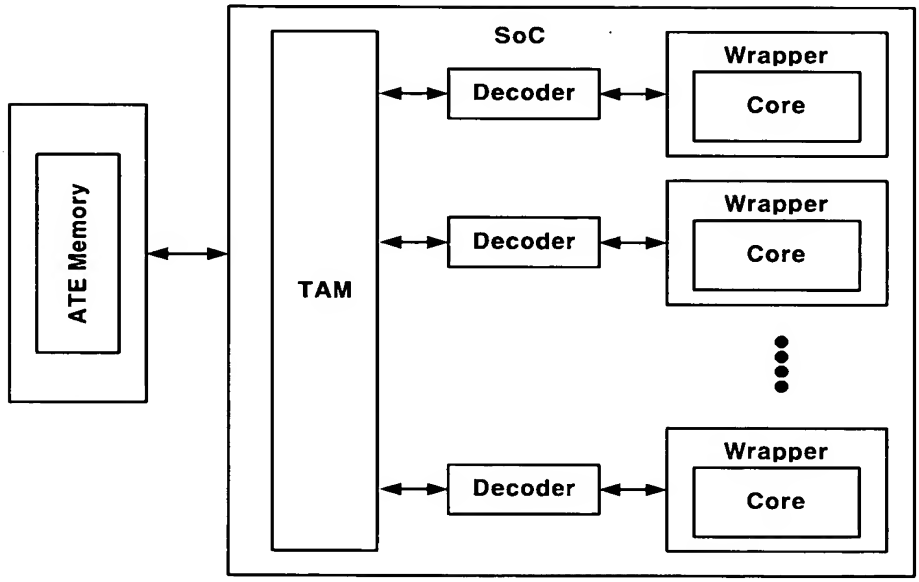
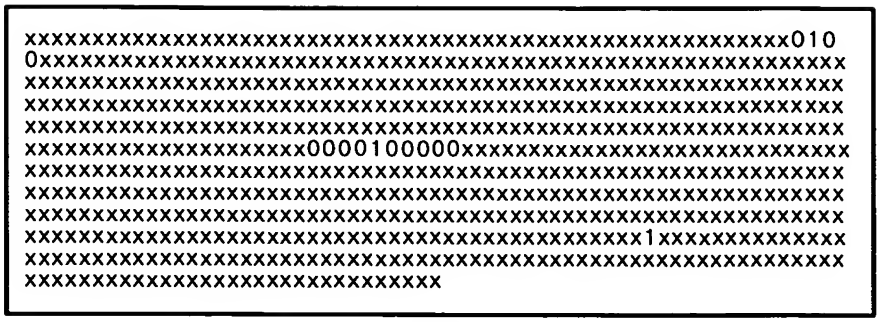
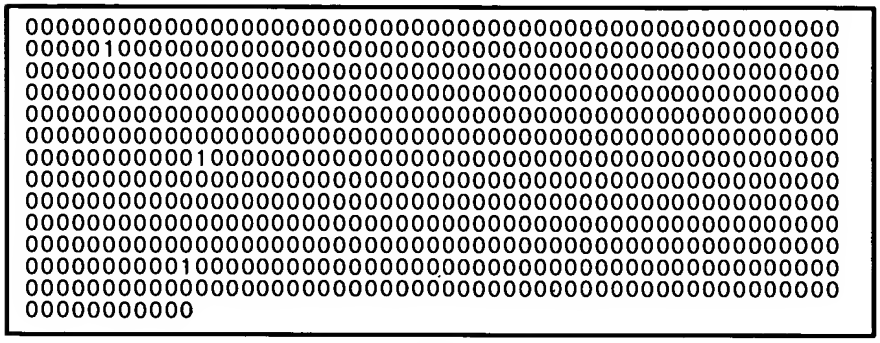


Fig. 4



(a)



(b)

Fig. 5a

Pattern	Herfman Code	Patter	MSCIR
0000	10	0000	0
0100	00	00	100
0010	110	01	101
0001	010	10	110
1000	0110	11	111

Fig. 5b

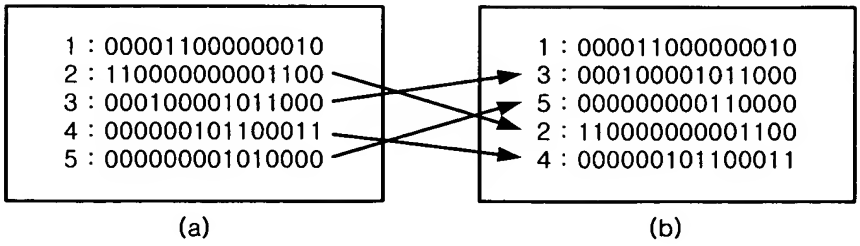


Fig. 6

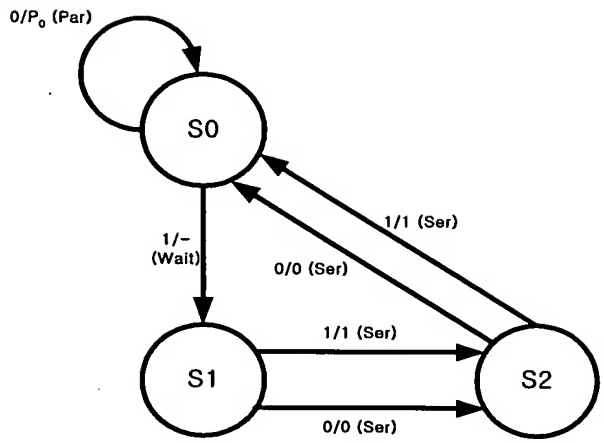

0/P0 (Par)
S0
1/-
(Wait)
0/0 (Ser)
1/1 (Ser)
S1
S2
1/1 (Ser)
0/0 (Ser)

Fig. 7

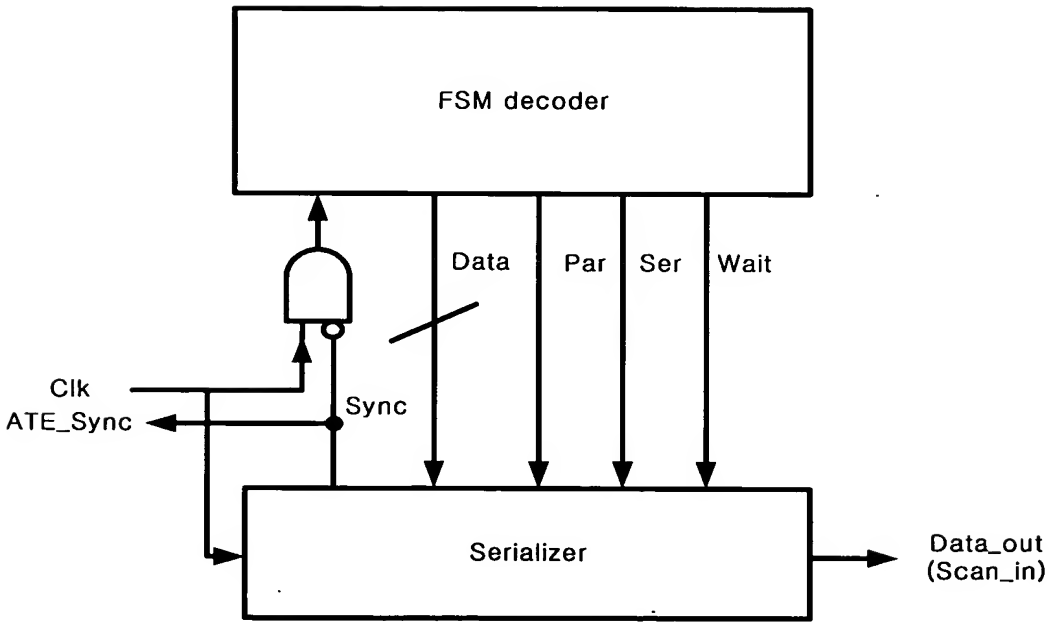

FSM decoder
Data
Par
Ser
Wait
Clk
ATE_Sync
Sync
Serializer
Data_out
(Scan_in)

Fig. 8